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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/025,553	12/26/2001	Llewellyn Yance	P21848	8319

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EXAMINER	
PARK, EDWARD K	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 03/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/025,553	YANCE ET AL.	
	Examiner	Art Unit	
	Edward K. Park	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *030305*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bui (U.S. 6,763,478) in view of Arai (U.S. 5,978,922). Claim rejections from previous Office Action are reproduced below for Applicants' convenience.

With respect to claim 1, Bui discloses a method for controlling a microcomputer in a microcomputer system (column 3, lines 60-61) with a high speed operation mode and a low speed operation mode (column 3, lines 60-64) in which the low speed of the microcomputer is slower than that of the high speed operation mode, the microcomputer system including a clock operable in the high and the low speed operation modes (column 4, line 65 through column 5, line 2) and a backup power supply for supplying the clock with power for a predetermined time (column 3, lines 62-63), said method comprising: detecting power shutdown (column 4, lines 27-30); and switching from the high speed operation mode to the low speed operation mode (column 3, lines 36-39). Bui fails to disclose determining whether power is recovered within a given period; and setting the high speed operation mode when the power is determined to be recovered. Arai teaches a method for controlling a microcomputer system that functions in a high speed operation mode and a low speed operation mode (column 5, lines 28-30) with a

backup power supply (column 3, lines 58-59), said method comprising steps of detecting power shutdown (column 6, lines 31-32), similar to Bui. Arai teaches the method further comprising determining whether power is recovered within a given time period (column 3, lines 31-33); and setting the high speed operation mode when power is determined to be recovered (column 3, lines 33-37) so that "[t]he last operating conditions of the computer system can be resumed within a short time" (column 3, lines 33-35). At the time the invention was made, it would have been obvious to a person of ordinary skill in the art, having references Bui and Arai in front of them, to combine the disclosure of Bui's variable clock speed system with the teachings of Arai's speed control and power resumption. The motivation for doing so would have been for an expedient recovery of the last operating conditions of the system.

With respect to claim 2, Arai further teaches the method for controlling a microcomputer according to claim 1 wherein the clock measures the given time period in the low speed operation mode (column 7, line 44-45).

With respect to claim 3, Arai further teaches the method for controlling a microcomputer according to claim 1, further comprising setting the microcomputer to a stop operation mode to stop operation unless the power is recovered within the given time period (column 7, lines 58-61).

With respect to claim 6, though Arai does not expressly teach that the second given time period is set to be longer than the first given time period by substantially an integral multiple. However, due to the finite precision of the clock frequency upon which the first given time period is dependent, the second given time period would necessarily

have to be set to substantially an integral multiple greater than the first given time period.

Claims 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bui (U.S. 6,763,478) in view of Arai (U.S. 5,978,922), and in further view of Klein (U.S. 6,178,523). Claim rejections from previous Office Action are reproduced below for Applicants' convenience.

With respect to claim 5, Bui discloses a method for controlling a microcomputer in a microcomputer system (column 3, lines 60-61) with a high speed operation mode and a low speed operation mode (column 3, lines 60-64) in which the low speed operation mode is slower than that of the high speed operation mode, the microcómputer system including a clock operable in the high and the low speed operation modes (column 4, line 65 through column 5, line 2) and a backup power supply for supplying the clock with power for a predetermined time (column 3, lines 62-63), said method comprising: detecting power shutdown (column 4, lines 27-30); and switching from the high speed operation mode to the low speed operation mode (column 3, lines 36-39). Bui does not disclose periodically determining whether power is recovered within a first given time period. Bui also fails to disclose switching to the high speed operation mode when the power is determined to be recovered; and setting the microcomputer to a stop operation mode to stop operation of the microcomputer unless the power is recovered within a second given time period which is longer than the first given time period. Arai teaches a method for controlling a microcomputer system that functions in a high speed operation mode and a low speed operation mode

(column 5, lines 28-30) and a backup power supply (column 3, lines 58-59), said method comprising: detecting power shutdown (column 6, lines 31-32), similar to Bui. Arai teaches the method further comprising determining whether power is recovered within a first given time period (column 3, lines 31-33); switching to the high speed operation mode when power is determined to be recovered (column 3, lines 33-37); and setting the microcomputer to a stop operation mode to stop operation of the microcomputer unless the power is recovered within a second given time period (column 7, lines 58-61). Arai does not teach periodically determining whether power is recovered within a first given time period. Klein teaches a method for controlling a microcomputer in a microcomputer with a high speed operation mode and low speed operation mode, and a backup power supply, similar to Bui and Arai. Klein teaches the method further comprising periodically determining whether power is recovered within a first given time period (column 6, lines 5-13) in order to conserve power by determining the earliest point of possible power shutdown recovery. Arai does not expressly teach that the second time period is longer than the first given time period. However, in order for Arai's method to function properly, the second time period would have to necessarily be longer than the given first time period determined by the frequency of the clock in the low speed operation mode in order to properly detect shutdown recovery. At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the disclosure of Bui's variable clock speed system with the teachings of Arai's speed control and power resumption and Klein's periodic recovery checking. The motivation for doing so would have been for an expedient recovery of the last operating

conditions of the system and to determine the earliest possible point at which the high speed operation mode could be restored, saving time and the life of the backup power supply.

With respect to claim 8, Bui discloses a method for controlling a microcomputer in a microcomputer system (column 3, lines 60-61) with a high speed operation mode and a low speed operation mode (column 3, lines 60-64) in which the low speed operation mode of the microcomputer is slower than that of the high speed operation mode, said microcomputer system including a clock operable in the high and the low speed operation modes (column 4, line 65 through column 5, line 2) and a backup power supply for supplying the clock with power for a predetermined time (column 3, lines 62-63), said method comprising: detecting power shutdown (column 4, lines 27-30); and switching from the high speed operation mode to the low speed operation mode when the clock is set (column 3, lines 36-39). Bui does not disclose checking whether the clock is set or setting the microcomputer to a stop operation mode to stop operation of the microcomputer unless the clock is set. However, it would have been obvious to one skilled in the art at the time of the invention that if the clock were not set, the microcomputer would have to be set to a stop operation mode since it would not be available to operate in either the low or high speed operation modes. Bui fails to disclose periodically determining whether the power is recovered within a first given time period. Bui also does not disclose switching to the high speed operation mode when the power is determined to be recovered; and setting the microcomputer to a stop operation mode to stop operation of the microcomputer unless the power is recovered

within a second given time period which is longer than the first given time period. Arai teaches a method for controlling a microcomputer in a microcomputer system with a high speed operation mode and a low speed operation mode (column 5, lines 28-30) and a backup power supply (column 3, lines 58-59), said method comprising: detecting power shutdown (column 6, lines 31-32), similar to Bui. Arai teaches the method further comprising determining whether the power is recovered within a given first time period (column 3, lines 31-33); switching to the high speed operation mode when the power is determined to be recovered (column 3, lines 33-37); and setting the microcomputer to a stop operation mode to stop operation unless the power is recovered within a second given time period (column 7, lines 58-61). Arai does not teach periodically determining whether the power is recovered within a first given time period. Klein teaches a method for controlling a microcomputer in a microcomputer system with a high speed operation mode and low speed operation mode, and a backup power supply, similar to Bui and Arai. Klein teaches the method further comprising periodically determining whether the power is recovered within a first given time period (column 6, lines 5-13) in order to conserve power by determining the earliest point of possible power shutdown recovery. Arai does not expressly teach that the second time period is longer than the first given time period. However, in order for Arai's method to perform properly, the second time period would have to necessarily be longer than the given first time period determined by the frequency of the clock in low speed operation mode in order to properly detect shutdown recovery. At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the disclosure of Bui's variable clock speed system

with the teachings of Arai's speed control and power resumption. The motivation for doing so would have been for an expedient recovery of the last operating conditions of the system and to determine the earliest possible point at which the high speed operation mode could be restored, saving time and the life of the backup power supply.

Claims 4, 7, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bui (U.S. 6,763,478) in view of Kohn (The IEEE Standard Dictionary of Electrical and Electronics Terms, 6th ed.) and Arai (5,978,922). Claim rejections from previous Office Action are reproduced below for Applicants' convenience.

With respect to claim 4, Arai further teaches the method for controlling a microcomputer according to claim 1, further comprising storing a value representing a time period, which the microcomputer measures during power shutdown (column 7, lines 58-61). Arai fails to explicitly teach storing the value representing said time period in volatile memory of the microcomputer system. However, it is well known in the art that counters are used to store values representing time periods. Kohn defines a counter as "A device such as a register or storage location used to represent the number of occurrences of an event" (page 228). As registers are a type of volatile memory, the value representing the time period would necessarily have to be stored in volatile memory of the microcomputer system.

With respect to claim 7, Arai further teaches the method for controlling a microcomputer according to claim 5, further comprising storing a value representing a time period which the microcomputer measures during power shutdown (column 7, lines 58-61). Arai fails to explicitly teach storing the value representing said time period in

volatile memory of the microcomputer system. However, it is well known in the art that counters are used to store values representing time periods. Kohn defines a counter as "A device such as a register or storage location used to represent the number of occurrences of an event" (page 228). As registers are a type of volatile memory, the value representing the time period would necessarily have to be stored in volatile memory of the microcomputer system.

With respect to claim 9, Arai further teaches the method for controlling a microcomputer according to claim 8, further comprising storing a value representing a time period which the microcomputer measures during power shutdown (column 7, lines 58-61). Arai fails to explicitly teach storing the value representing said time period in volatile memory of the microcomputer system. However, it is well known in the art that counters are used to store values representing time periods. Kohn defines a counter as "A device such as a register or storage location used to represent the number of occurrences of an event" (page 228). As registers are a type of volatile memory, the value representing the time period would necessarily have to be stored in volatile memory of the microcomputer system.

Response to Arguments

2. All rejections of claim limitations as filed prior to Amendment dated March 03, 2005 not argued in their entirety or substantively in the response to the prior Office Action have been conceded by Applicants, and the rejections are maintained henceforth.

Applicant's arguments filed March 03, 2005 have been fully considered but they are not persuasive.

In response to Applicants' argument that there is no suggestion to combine the references, the Examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case of Bui and Arai, the motivation to combine the teachings of Bui's variable clock speed system and Arai's speed control and power resumption lies in the expedient recovery of the last operating conditions of the system, as taught by Arai (column 3, lines 1-4). Further, the motivation to combine the teachings of Bui and Arai with Klein's periodic recovery checking lies in the ability to determine the earliest possible point at which the high speed operation mode could be restored, saving time and the life of the backup power supply, as taught by Klein (column 2, lines 46-56).

With regards to Applicants' assertions arguing the lack of mention of detecting power shutdown in Bui, the Examiner directs Applicants to column 4, lines 27-30 of Bui, which discloses: "A transition change may be initiated by the OS by detection of a change from battery to AC, or from AC to battery power, in essence plugging or unplugging an AC connector from the system." The phrase "power shutdown" in claim 1

is interpreted as a removal of power, demonstrable from in essence unplugging an AC connector from the system. Therefore, the rejection for claim 1 is proper.

With regard to Applicants' assertions arguing the lack of disclosure of periodically determining whether power is recovered within the predetermined time period in Klein, the Examiner directs Applicants to column 6, lines 5-13 of Klein, which states: "...it is tested whether the interrupt is present for a predetermined time period TT, for example 2 seconds." Given that testing for the presence of the interrupt is a continual process throughout the duration of the predetermined time period TT, and that all operation within the microcomputer system is dictated by a periodic clock frequency, Klein must necessarily provide periodic determination of the presence of the reconnect main power interrupt signal (column 6, lines 12-13). Therefore, the rejections for claims 5 and 8 are proper.

Accordingly, Applicants' assertions concerning the rejections of dependent claims 2-4, 6-7, and 9 are invalid, as the rejections of their respective independent claims 1, 5, and 8 are proper.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward K. Park whose telephone number is (571) 272-5859. The examiner can normally be reached on M-F, 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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